WHAT IS CLAIMED IS:

1. A method of operating an integrated circuit including read accessible memory comprising the steps of:

testing memory read operations beginning at a maximum speed at successively slower speeds until all memory reads pass;

determining memory read program bits for a highest memory speed passing the memory read tests; and

programming write once bits according to determined memory read program bits.

2. The method of claim 1 further comprising the steps of:

preliminary soft programming determined bits; and

testing non-memory portions of the integrated circuit using soft programmed determined memory read program bits.

3. The method of claim 1 wherein:

said step of programming write once bits includes

applying program voltages to the bits,

testing the write once bits to determine achieved programming, and

repeating applying program voltages and testing the write once bits until the testing confirms correct write once bit programming.

4. The method of claim 1 wherein programming of eFuse bits includes:

merging of programming of write once bits for memory read speed with programming write once bits not related to memory speed.

5. The method of claim 4 wherein:

the write once bits not related to memory speed include a specific die-identification bit code.

6. The method of claim 4 wherein:

the write once bits not related to memory read speed include write once bits for memory redundancy programming.

7. The method of claim 4 wherein:

the write once bits not related to memory read speed include write once bits for control of programmable logic functions.

8. The method of claim 1, wherein the read accessible memory is write accessible, further comprising:

testing memory write operations beginning at a maximum speed at successively slower speeds until all memory reads pass;

determining memory write program bits for a highest memory speed passing the memory write tests; and

said step of programming write once bits according to determined memory read program bits further includes programming write once bits according determined memory write program bits.

9. A method of operating an integrated circuit including write accessible memory comprising the steps of:

testing memory write operations beginning at a maximum speed at successively slower speeds until all memory writes pass;

determining memory write program bits for a highest memory speed passing the memory write tests; and

programming write once bits according to determined memory write program bits.

10. The method of claim 9 further comprising the steps of:

preliminary soft programming determined write once bits; and

testing non-memory portions of the integrated circuit using soft programmed determined memory write program bits.

11. The method of claim 9 wherein:

said step of programming write once bits includes

applying program voltages to the write once bits,

testing the write once bits to determine achieved programming, and

repeating applying program voltages and testing the write once bits until the testing confirms correct write once bit programming.

12. The method of claim 9 wherein:

programming of write once bits includes merging of programming of write once bits for memory write speed with programming write once bits not related to memory speed.

13. The method of claim 12 wherein:

the write once bits not related to memory write speed include a specific die-identification bit code.

14. The method of claim 12 wherein:

the write once bits not related to memory write speed include write once bits for memory redundancy programming.

15. The method of claim 12 wherein:

the write once bits not related to memory write speed include write once bits for control of programmable logic functions.

16. An integrated circuit comprising:

a plurality of write once bits including at least one read timing write once bit and at least one write timing write once bit;

a logic circuit;

a read/write memory connected to said write once bits and said logic circuit, said read/write memory operable to read data from memory locations specified by said logic circuit and write data to memory locations specified by said logic circuit, said read/write memory including

a read timing circuit selecting one of a plurality of intervals of time from a start of read operations until sampling of read data dependent upon said at least one read timing write once bit, and

a write timing circuit selecting one of a plurality of intervals of time of application of write data to said corresponding memory locations dependent upon said at least one write timing write once bit.

17. The integrated circuit of claim 16, wherein:

said logic circuit includes a programmable data processor.

18. The integrated circuit of claim 16, further comprising:

a plurality of data bit latches, one data bit latch corresponding to each of said write once bits;

wherein said reading timing circuit is responsive to said data bit latches corresponding to said at least one read timing write one bit in a test mode; and

wherein said write timing circuit is responsive to said data bit latches corresponding to said at least one write timing write one bit in a test mode.